THE CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a plurality of logic areas, the plurality of logic areas comprising an array of logic-gates or logic-blocks or custom logic which form functional blocks; and an actively switchable network selectively connecting one logic area with another logic area;

wherein the integrated circuit provides a chip-architecture where the functional blocks are specific hardware functional blocks, hardware functional blocks that are parameterized, and/or programmable functional blocks including programmable processors; and

further wherein the functional blocks act as objects requesting and providing services to other objects on the actively switchable network, and when a functional block is a programmable processor the functional block optionally implements objects, the programmable processor making one, some or all objects thereof visible to other objects connected to the actively switchable network.

2. The integrated circuit of claim 1, wherein the integrated circuit provides a particular object or logic that is responsible for receiving requests for services and for providing an address of an object that provides the required service.

3. The integrated circuit of claim 1, wherein the integrated circuit provides at least one client object and at least one service object each of predetermined location which are fixed.

4. The integrated circuit of claim 1, wherein locations of objects are determined when the objects are loaded into field programmable gate arrays (FPGA), or at least one programmable processor, loader circuitry applying where objects are to be placed on a target device, a map being used to specify connections between objects whilst loading.

5. The integrated circuit of claim 1, wherein objects are loaded onto a target device without interconnection therebetween and, in use, when a client object requires a service other objects are broadcast a request to provide such a service, service objects capable of providing the service responding to the client object, and a service object selected as the chosen service object by the client object, and interconnection defined between the client object and chosen service object.

6. The integrated circuit of claim 1, wherein objects are loaded onto a target device without interconnection therebetween and, in use, objects broadcast services which can be provided and other objects record a location of the objects providing services which will be required.

7. The integrated circuit of claim 1, wherein the integrated circuit provides an object cache where an object is loaded temporarily when required to perform a service and moved to an external memory when services are no longer required.

8. The integrated circuit of claim 1, wherein the integrated circuit provides an object cache where an object is loaded temporarily over an external network when required to perform a service and means for returning the object over the external network when services are no longer required.

9. The integrated circuit of claim 7, wherein an object cache operates with a fixed set of functional blocks held permanently in the object cache and where specific instances are held in external memory and loaded when needed.

10. The integrated circuit of claim 9, wherein instance memory that holds only instances of a particular object type is provided adjacent to the functional block implementing that particular type of object.

11. The integrated circuit of claim 7, wherein there is provided a plurality of object cache controllers.

12. The integrated circuit of claim 1, wherein the integrated circuit is fabricated in a semi-conductor material such as Silicon (Si).

13. The integrated circuit of claim 1, wherein a given logic area comprises a single physical area of the integrated circuit or comprises a plurality of discrete areas of the integrated circuit.

14. The integrated circuit of claim 1, wherein the actively switchable network comprises an on-chip packet switching network.

15. The integrated circuit of claim 14, wherein the packet-switching network includes interfaces for connecting functional blocks to the network, routing switches, and point-to-point links between interfaces and routing switches and between routing switches and other routing switches.

16. The integrated circuit of claim 1, wherein signals are effectively connected between functional blocks by taking a present value of one or more signals at a source functional block, packing these value(s) as data into a packet cargo and sending a packet across the on-chip network, a header for the packet being set to contain a location of a destination functional block, and when the packet arrives at a destination, appropriate signals within the destination functional block are set to values defined in the packet cargo.

17. The integrated circuit of claim 16, wherein each network interface contains a means of packing signals into packets, a transmitter for sending packets, a receiver for receiving packets and a means of extracting signal(s) from the packet.

18. The integrated circuit of claim 16, wherein the packet-switching network transports packets from an interface connected to signal source(s), across selected links and routing switches making up the network, to an interface connected to a signal destination functional block, each packet comprising a header, a cargo and a delimiter, the header defining a location of the destination for the packet, the cargo containing data or signal values to be sent across the network, the delimiter separating one packet from another.

19. The integrated circuit of claim 18, wherein packets are delimited by a start of packet marker or by an end of packet marker, the start of packet marker and/or

end of packet marker being special codes added by a link transmitter at a start or end of a packet that a link receiver recognizes.

20. The integrated circuit of claim 18, wherein packets are sent without a delimiter in which case either packets are of a known fixed length or information is added to a packet header, which details a length of a packet.

21. The integrated circuit of claim 18, wherein where there is more than one link connecting a pair of routing switches, the links comprise equivalent routes for a packet, so any one of the links may be used to forward a packet, such that when a new packet arrives at a routing switch to be sent to a particular destination, if one link is already busy sending another packet then the new packet can be sent out of one of the other equivalent links.

22. The integrated circuit of claim 18, wherein the actively switchable network is selected from a construction comprising:

a network that switches packets of information using routing switches arranged in a substantially regular grid;

a network that switches packets of information using routing switches arranged irregularly;

a network that uses a physical location of a destination logic area to determine the routing through the network.

a network that uses a name of the destination logic area to determine routing through the network where each routing switch has a look up table to translate from the name to an output port that a packet is to be forwarded through;

a network where packet destinations are specified as a route or collection of possible routes through the network;

a network where packets are sent from one routing switch to a next in a ring or loop eventually returning back to a source of the packet, wherein a user logic area accepting the packet removes the packet from the loop, and the accepting user logic area puts a reply onto the loop so that it moves on round the loop until it arrives back at a source of the original packet where it is received and removed from the loop; or

a network which uses a combination of routing switch arrays and loops.

23. The integrated circuit of claim 1, wherein different functional blocks operate asynchronously or synchronously one with the other.

24. The integrated circuit of claim 23, wherein when operating asynchronously, a source functional block requests a service from another functional block by sending the another functional block a message, and the source functional block suspends operation until the source functional block receives a response from a requested service or the source functional block continues doing other operations until the source functional block can proceed no further without a response, when a message arrives at the another functional block or a target block providing the requested service, the service is actioned and the response returned to the functional block that requested the service, the source functional block then continues with its operation, requesting and providing services to other blocks as necessary.

25. The integrated circuit of claim 24, wherein the functional blocks operate asynchronously with synchronization between blocks occurring only when some exchange of information has to take place.

26. The integrated circuit of claim 23, wherein when operating synchronously, signal values are transferred from a source functional block to a destination functional block and be held in a synchronization register, a synchronization signal then updates the destination functional block with new signal values and packets of signal values are sent to appropriate destinations from all sources that have modified their output values since the last synchronization signal.

27. The integrated circuit of claim 26, wherein operation comprises the steps of:

(1) on receiving a synchronization signal all input signals are updated with new values from the synchronization register,

(2) each logic block propagates these new input signals through to produce an output signal,

(3) the new output signal values are put in packets and sent to required destination blocks, and

(4) the synchronization signal is asserted and the process continues.

28. The integrated circuit of claim 27, wherein a single synchronization signal synchronizes a plurality of logic blocks, computation and distribution of new signal values being complete before a next time the synchronization signal is asserted.

29. The integrated circuit of claim 27, wherein several different synchronization signals are used, with a period of the synchronization signal being matched to a required performance of each logic block, the synchronization period being long enough to allow all the relevant signals and data to be transferred in packets to their required destinations before the next synchronization signal.

30. The integrated circuit of claim 1, wherein the integrated circuit provides a chip architecture including an actively switchable network which is extended off-chip to provide for inter-chip communication, an off-chip extension of the on-chip network using single-ended or differential signalling for a link between the chip and another chip(s), the off-chip extension incorporating error correction/detection coding within each packet.

31. The integrated circuit of claim 1, wherein the integrated circuit provides a chip architecture in which an interface to the functional-blocks takes the form of an operation identifier, followed by a set of parameters, each functional block implementing one or more operations, the operation identifier selecting which operation a functional-block is to perform, the set of parameters containing those pieces of information that an operation requires in order to fulfill a task thereof; distinct functional-blocks or "objects" with well-defined functionality, collaborating to provide required system-level functionality, each object providing specific functionality, defined by the operations supported thereby, collaboration between the objects being supported by message passing between objects to allow one object to request an operation or service from another object, the infrastructure to support message passing being provided by the on-chip network, operation requests and associated parameters being transformed by the network interface to the signals and data values that the functional-block (object) needs to carry out the requested operation.

32. The integrated circuit of claim 31, wherein a message is either a service request or a reply to a service request, a service request message comprising source and destination object identifiers, operation identifier, and parameters, a reply comprising source and destination identifiers, operation identifier and result data or acknowledgement.

33. The integrated circuit of claim 32, wherein each message is placed in a single packet or a message is split over several smaller packets.

34. The integrated circuit of claim 1, wherein programmable processors that execute out of local cache memory obtaining program code and/or data via the on-chip network from other memory areas when there is a cache miss.

35. The integrated circuit of claim 1, wherein error detection or correction is added to data/control characters or packets to improve reliability in situations where there are single event upsets within the chip.

36. The integrated circuit of claim 1, wherein to reduce power consumption a link is stopped when the said link no longer has any information to send, the link only sending data or control characters when there are characters to send otherwise it is not active.

37. An integrated circuit providing a plurality of interconnections between distinct defined areas of the integrated circuit, each interconnection comprising one or more serial links, each serial link having at one end thereof means for transmitting a plurality of parallel signals serially along the said serial link, and at another end thereof means for receiving the serially transmitted plurality of parallel signals, wherein further the integrated circuit provides means for reconstructing the plurality of parallel signals from the serially transmitted plurality of parallel signals.

38. An integrated circuit comprising:

a plurality of logic areas; and

an actively switchable network selectively connecting one logic area with another logic area.

39. A system or an apparatus including an integrated circuit according to claim 1.

40. An assembly comprising at least two integrated circuits according to claim 1, including means for transferring data between the at least two integrated circuits.

41. A method of communication within an integrated circuit comprising the steps of:

providing an integrated circuit according to claim 1;

selecting a source logic area from the plurality of logic areas;

selecting a destination logic area from the plurality of logic areas;

encoding data from the source logic area as a data packet;

transmitting said data packet from the source logic area to the destination logic area via actively switchable network; and

decoding the data at the destination logic area from the data packet.

42. An integrated circuit having an architective comprising arrays of logic-gates or logic-blocks and an on-chip packet-switching network.